Remarks

Claims 1-4, 6-9, 11-14 and 16 are currently pending in the patent application. For the reasons and arguments set forth below, Applicant respectfully submits that the claimed invention is allowable over the cited references.

The Office Action dated April 17, 2008 indicated an objection to claims 6, 11 and 16 and listed the following rejections: claims 6, 11 and 16 stand rejected under 35 U.S.C. § 112, second paragraph; claims 1-4, 7-9 and 12-14 stand rejected under 35 U.S.C. § 102(b) over Nogradi (U.S. Patent No. 5,974,518); claims 1, 6, 7, 11, 12 and 16 stand rejected under 35 U.S.C. § 103(a) Shemla *et al.* (U.S. Patent No. 5,809,557) in view of Brown *et al.* (U.S. Patent No. 5,916,309).

Applicant respectfully traverses the rejection and objection (each relying upon the same rationale) of claims 6, 11 and 16. As pointed out by the Examiner and as would be recognized by the skilled artisan, N and M represent variables (this contradicts the Examiner's statement that it is unclear what N and M represent). The skilled artisan would recognize, as the Examiner has, that N and M represent numerical variables. Whether or not N and M are limited to positive integers or some other class of variables is an aspect that relates to the breadth of the claims. As stated in M.P.E.P. § 2173.04, breadth is not indefiniteness:

> Breadth of a claim is not to be equated with indefiniteness. *In re Miller*, 441 F.2d 689, 169 USPQ 597 (CCPA 1971). If the scope of the subject matter embraced by the claims is clear, and if applicants have not otherwise indicated that they intend the invention to be of a scope different from that defined in the claims, then the claims comply with 35 U.S.C. 112, second paragraph.
> M.P.E.P. § 2173.04

In connection with the scope of claims 6, 11 and 16, N and M represent variables and, more particularly, they represent bits. The Examiner's erroneous request to narrow the claims to a specific type of variable (such as an integer) is an improper use of 35 U.S.C. 112, second paragraph, to limit the breadth of the claim. Notwithstanding, Applicant has amended the claims to indicate that N and M are positive integers. Accordingly, Applicant respectfully requests that the rejection and objection be withdrawn.

Applicant respectfully traverses the Section 102(b) rejection of claims 1-4, 7-9 and 12-14 because the cited portions of the Nogradi reference do not correspond to the claimed invention. Applicant notes at the outset that teachings of the Nogradi reference relied upon in the rejection are directed to a set of buffers for storing Ethernet frames. As indicated in the Abstract, frames smaller than the buffer size result in wasted buffer space. This implies that an individual buffer does not store more than a single Ethernet frame. Also of note is that the buffer descriptor 36 includes information regarding the length of the message in the buffer. This implies that circular queuing is not used within each buffer. Thus, unlike embodiments of Applicant's invention, the Nogradi reference does not teach such circular queuing within a buffer.

Turning now to the specifics of the claim limitations, Applicant notes that the claims include limitations directed to providing circular access to/within a buffer. Moreover, Applicant has made amendments with limitations directed to sets of buffers and that each set is accessed using circular-access to or within the set. To the extent that Nogradi discloses circular access, the circular access is related to buffer descriptor 36 and does not pertain to access to sets of the buffers (*e.g.*, the circular access is to a table describing the contents of a particular buffer and not to accesses made within the buffer). Applicant respectfully submits that the "circular queue" of the Nogradi reference is with respect to access to the full set of buffers, whereas Applicant's claim limitations are directed to a circular buffer function within a selected buffer. Accordingly, the rejection of each of the claims is improper.

Furthermore and with particular regard to claim 2, Applicant submits that the Nogradi reference fails to teach correspondence to each claim limitation. The Office Action relies upon the pointer 51 of FIG. 2 and related discussion to show correspondence to various limitations directed to a circular-increment function. Applicant respectfully submits that the "circular queue" of the Nogradi reference is with respect to access to the full set of buffers, whereas Applicant's claim limitations are directed to a circular buffer function within a selected buffer. Applicant submits that the claim language indicated that the pointer was to a select buffer of the plurality of buffers. Applicant has made amendments that explicitly state that the circular-increment function

is relating to locations within the select buffer, rather than to each different buffer. These amendments were not intended to change the scope of the claim.

Applicant further submits that the Office Action has relied upon the increment function to correspond to two different limitations (increment function and over-write function), thereby effectively reading out one of the limitations. Notwithstanding, Applicant has amended the claim limitations to recite that the overwrite function is directed to bits that differentiate the select buffer from others of the plurality of buffers and not to bits indicating a location within the buffer. Accordingly, the Nogradi reference fails to teach correspondence to each of the claim limitations and Applicant respectfully requests that the rejection be withdrawn.

With particular regard to claim 7, Applicant respectfully submits that the Office Action has improperly pieced elements together in a manner not taught by the Nogradi reference. The Office Action appears to rely upon buffers 1-N of FIG. 2 in attempting to show correspondence to claim 7. The Office Action, however, relies upon teachings relating to circular access to receive buffer descriptor table 38 when discussing the circular queue. Applicant notes that claims 7 and 9 are directed to the same buffer, and thus, correspondence cannot be shown by teachings relating to two distinct buffers. In particular, the Office Action has not shown (and Nogradi does not appear to teach) correspondence to circular access to buffers 1-N. Accordingly, Applicant respectfully submits that the rejection is improper and requests that it be withdrawn.

Applicant respectfully traverses the Section 103(a) rejections of claims 1, 6-7, 11-12 and 16 (each of which is based upon Shemla in view of Brown) because there is no reason to combine the references in the manner asserted by the Office Action. The Office Action incorrectly reasons that because the claims do not require dynamically portioning of the memory, the combination does not either. Applicant respectfully submits that the partitioning cannot be static if the partitioning is somehow responsive to parameters received from an application. Moreover, neither of the references teaches how the circuit of Shemla would be modified to allow for such a response to the application provided parameters.

Applicant respectfully submits that the Office Action's reasoning provides evidence of an improper analysis of the references. The test for obviousness should rely

upon an analysis of what the references teach and should not be tainted knowledge gleaned only from applicant's disclosure. *See, e.g.*, M.P.E.P. 2145. Applicant respectfully submits that a proper analysis of the elements shows that the determination of the number of partitions is implemented in response to a parameter received from an application. The Office Action asserts that the determination is not dynamic, in part, because the claims do not require it to be dynamic. Applicant's argument was not directed to claim limitations and instead provided an analysis of the teachings of the references and the asserted combination. Thus, the Office Action has improperly used Applicant's claims to discount evidence suggesting that the skilled artisan would not look to combine the elements as suggested by the Office Action. The substance of Applicant's previous discussion is reproduced below for convenience.

The Office Action asserts that it would be obvious to modify the circuit of Shemla to partition the memory based on a partitioning parameter as taught by Brown for the benefit of improved memory utilization. This combination overlooks the context of the references and results in an illogical combination. More specifically, the Shemla reference is directed to a hardware-implemented multiple FIFO array that includes memory (12) being partitioned into N sections with N write pointer registers (18) each corresponding to one of the N FIFOs. A write MUX (14) with N write inputs is coupled to each of the N write pointer registers (18). *See, e.g.,* FIG. 1 and Col. 1:34-57. The Examiner's asserted combination attempts to make the number partitions N a dynamically adjustable variable. Applicant respectfully submits that neither reference teaches or suggests that such dynamic allocation is possible in the hardware implementation of the Shemla reference. For example, Shemla's multiple FIFO array is designed with a fixed number of partitioned sections N, with a corresponding number of write pointer registers and read pointer registers required to access each of the partitioned sections N. While different circuits may contain a different number of partitioned sections from one another, any one circuit has a fixed number of partitioned sections. As such, the circuit taught by Shemla is not capable of dynamically partitioning the memory and would be incompatible with the partitioning parameter as taught by Brown because the general discussion of the Brown reference does not teach or suggest any circuit that would function with the cited circuit of the Shemla reference.

Thus, Applicant submits that the Office Action has merely identified elements of two references without viewing the combination of references "as a whole", as expressly stated in 35 U.S.C. § 103(a). Applicant respectfully submits that the Office Action cannot merely pluck an element defined as a vague conceptual idea, such as memory partitioning, without assessing how the element would function with the underlying circuit. "The MPEP explains that all the limitations in a claim are to be considered, even if such language is purely functional as "the claims must be given full weight and may not be disregarded in evaluating the patentability of the subject matter defined employing such functional language." Ex parte Bylund, 217 U.S.P.Q. 492, 498 (Bd. Pat. App. 1981); See also, In re Venezia, 530 F.2d 956, 189 U.S.P.Q. 149 (CCPA 1976) and MPEP 2173.05(g); see also 35 U.S.C. 103(a) (requiring consideration of the claim "as a whole")."

Moreover, such an assessment should be made without relying upon information gleaned only from Applicant's disclosure. Should the rejection be maintained, Applicant requests clarification as to how the vague concept of memory partitioning (in response to a parameter from an application) would be implemented in the circuit of Shemla.

In view of the remarks above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Peter Zawilski, of NXP Corporation at (408) 474-9063 (or the undersigned).

Please direct all correspondence to:

Corporate Patent Counsel
NXP Intellectual Property & Standards
1109 McKay Drive; Mail Stop SJ41
San Jose, CA 95131

CUSTOMER NO. 65913

By: _____
Name: Robert J. Crawford
Reg. No.: 32,122
651-686-6633
(NXPS.290PA)